A 10-bit 160-MSPS 2.5-V Segmented Current Steering CMOS DAC for WLAN Applications

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Abstract — This paper presents a 10-bit 160-MSPS 2.5-V digital to analog converter (DAC) and is implemented in TSMC 0.25µm CMOS technology. A segmented current steering architecture is used with optimized performance for speed, resolution, power consumption and area. The DAC can be operated up to 160MHz sampling frequency and the settling time is less than 4.8 ns. The differential nonlinearity (DNL) and integral nonlinearity (INL) are ±0.3 and ±0.4 least significant bits (LSBs), respectively. The spurious free dynamic range (SFDR) at 160-MSPS remains above 68 dB for input frequency up to 50 MHz. Total power dissipation is 45.3 mW with 2.5-V power supply. The chip size is 1.73 mm × 1.2 mm.

Key Words — CMOS, digital to analog conversion, mixed analog-digital integrated circuits.

I. INTRODUCTION
Recently, many of system such as Wireless LAN, DDS, AWG, HDTV require employing high performance DACs. Therefore, many of mixed signal IC design engineers have conducted researches on improvement of CMOS DAC. In these systems, the key performance parameters of the DAC are low power consumption, higher conversion rate, high resolution and small die area. Current steering DACs are based on an array of matched current sources which are binary weighted [1] or unary decoded [2]. For signal processing applications, the segmented architecture, that combines binary weighted and unary decoded current cells, is the most often used for the following reason: it allows a tradeoff of reduction in the glitch energy and differential nonlinearity, with an increase in the decoding logic complexity and the overall layout area.

802.11a and 802.11g are the most popular network standards in wireless LAN which have the data rate up to 54 Mbps and 20 MHz sampling rate. This paper proposes a 10-bit 160-MSPS DAC which suits with the specifications of the above-mentioned standards. System level analysis meet the requirement of 10-bit resolution and 68 dB SFDR when the input sinewave frequency is up to 50 MHz. The DAC is fabricated in TSMC 0.25 µm CMOS technology and the chip size is 1.73 mm × 1.2 mm. Total power dissipation is 45.3 mW with 2.5-V power supply.

The outline of the paper is as follows. In Section II, the basic operation principles of segmented current steering DAC and the topology selection are discussed. In Section III, the building blocks of the current steering DAC are covered in detail. The layout consideration is discussed in Section IV. Section V presents the results and Section VI summarizes the conclusions.

II. ARCHITECTURE DESIGN OF 10-BIT DAC

Fig. 1 shows a conceptual circuit of N-bit binary weighted DAC. The digital inputs (b0, b1, b2, ..., bN-2, bN-1) directly control the switches to determine the current value flowing into the output resistance. The virtues of this architecture are its simplicity, as no decoding logic is required and the small required silicon area. The major drawbacks are the sensitivity to device mismatch, and the finite output impedance of the current source for higher number of bits.

Fig. 2 shows a conceptual circuit of N-bit unary coded DAC. In the unary coded architecture, only one additional current source has to be switched to the output as the digital input increases a LSB. Hence, the analog output is always increased as the digital input increased. The monotonous property of the output signal is guaranteed. The advantages of this architecture are on its good DNL and greatly minimizing the glitch problem. The major drawbacks of this architecture are complexity, large area and more power consumption.
To get the best of both worlds, most current steering DACs are implemented using a segmented architecture. In this case, the DAC is divided into two sub-DACs: the B LSBs are implemented using a binary architecture and the (N-B) MSBs are implemented in a unary way. A theoretical analysis of method of proper segmentation is presented in [3]. A fully binary weighted design as 0% segmented, whereas a fully thermometer coded design is referred to as 100% segmented. This analysis discusses the minimization of chip area, under the constraints of true 10-bit dc performance, while simultaneously trying to optimize the frequency domain performance.

Fig. 3 shows the normalized required area versus percentage of segmentation [3]. X-axis represents the degree of segmentation and y-axis represents the current source area after normalization. Three dotted lines are the needed area of INL equal to 0.5 LSB, 1 LSB, 2 LSB which are independent of the amount of segmentation. Straight line from upper-left to lower-right represents the area at DNL equals to 0.5 LSB. Straight line from lower-left to upper-right represents the required digital circuit area.

As soon as the segmentation is less than 100%, glitches will contribute to distortion, particularly at higher frequency spectrum. Every additional bit in the LSB section will increase the distortion by 2 times. In this present application, 80% segmentation is chosen which implies 8 MSBs are implemented by thermometer coded DAC and 2 LSBs are implemented with binary weighted DAC. It can achieve 1.0 LSB INL, 0.5 LSB DNL, optimum chip area and total harmonic distortion.

III. DAC Building Blocks

A. Unit Current Cell

Fig. 5 shows the circuit of an unit current cell. It consists of a digital part and an analog part. The digital part consists of a decoding logic and a deglitch circuit. The decoding logic is equivalent to an AND-OR gate function and the deglitch circuit is essential for timing synchronization, as all the current cells should switch at the same time. The analog part consists of a differential cascode switch and a cascode current source.

The glitch is a major problem in unit current cell design. Glitch makes noise larger and affects circuit settling time. Some important issues [4] that have been identified to cause glitch are:

1) non-synchronization of input signal;
2) switches in the off-state at the same time;
3) coupling of the control signals through the $C_{GD}$ of the switches to the output;
4) output voltage variation of current source;

First, this problem was solved by placing a deglitch circuit in front of the switch. In this way, any delay introduced by the digital decoding logic can be circumvented. Second, this problem was solved by the use of two inverters. These circuits rise the cross point of the control signals of switches. As soon as one of the switching transistors begins to switch off, the complementary switching transistor starts to switch on. Third, this problem was solved by placing a cascode transistor on top of the switch. For a low-to-high transition of the control signal, while the switching transistor is forming a channel, the cascoded transistors are off and the signal path from the drain of the switching transistor to the output node is open. The coupling is therefore avoided. For a high-to-low transition, some coupling exists at the beginning. Since the switching transistor cuts off very rapidly, the voltage at the source of the cascode transistor drops, turning it off, and isolating the output node for the remaining of the transition of the control signals [5]. Fourth, this problem was solved by using cascode current source. This method can improve the input resistance of the current source, so
the output voltage variation can be suppressed.

B. Distributed Bias Circuit

DAC current source layout is always occupying large area. Only one bias circuit may cause the mismatch of the unit current cells. The principle of the distributed bias circuit is that the current is generated by bandgap circuit outside the current matrix and distributed to the surroundings of matrix. Current-mode distribution method can avoid the voltage drop on metal traces which will cause unit current cell mismatch. Fig. 6 shows the distributed bias circuit schematic. CS1 includes a bandgap reference circuit, folded cascode operation amplifier and current mirrors which generate a stable current independent of the temperature variation. Four times currents are mirrored from CS1 to CS2. CS3 is the circuit transfers the current to bias voltage in matrix. Each matrix needs four CS3, and there are sixteen CS3 in this DAC.

![Fig. 6 Distributed bias circuit and the current matrix.](image)

C. Global and Local Latch

Fig. 7(a) and (b) show the global and local latch circuits. In IC layout, there will be a long distance from PAD to decoding circuits. Global and local latch make digital signal synchronously input in decoding circuits.

Rising edge is used in global latch circuit design. When CLK=0, circuit is in hold mode and CLK=1, circuit is in evaluate mode. In local latch circuit design, falling edge is used. When CLK=0, circuit is in evaluate mode and CLK=1, circuit is in hold mode. The true single phase clock (TSPC) architecture is used in latch design to prevent the clock skew problem.

![Fig. 7 (a) Global latch. (b) Local latch.](image)

D. Thermometer Decoder

In thermometer coded DAC, binary inputs are converted into thermometer codes which are used for controlling the unit current cells. This thermometer decoder converts the M-MSBs of the binary code into \(2^M-1\) bits of the thermometer code representation. In the present design, 3-MSBs have been implemented by thermometer coded architecture. A binary-to-thermometer decoder with 3 binary input bits and 7 thermometer coded outputs is needed for direct implementation [6].

Fig. 8 shows the thermometer decoder circuits and implement in pull-down and pull-up couple network. In worst case, there will be at most three series transistors cost three times of rise time or fall time. However, it can satisfy the specification of 160 MHz sampling rate DAC and no need special structure of logic circuit.

![Fig. 8 Thermometer decoder circuits.](image)

IV. LAYOUT CONSIDERATION

For DAC with a resolution of 10 bits and higher, the dimensions of the current source array become so large that process, temperature and electrical gradients have to be considered. The nonlinearity errors introduced by these gradients can be compensated by special switching schemes [7].

A graphical representation of the double centroid switching structure of the current source array is given in Fig. 9. Each MSB unit current cell is delivering 4 times the LSB current. Each unit current cell is placed based on a centroid scheme in every quadrant. Since 63 unit current cells have to be placed in each quadrant, an 8 × 8 array is used. The four remaining places per quadrant are occupied by the LSBs. Four dummy rows and columns surrounding the 8 × 8 array have been added as to avoid edge effects. The shaded area represents the dummy cells.

![Fig. 9 Double centroid switching scheme.](image)
V. RESULTS

Two 50Ω double terminated load resistors are connected to the differential outputs and a 2.5-V supply. Fig. 10 shows the settling time performance of the DAC. The result shows that settling time is about 4.8 ns and the DAC can operate up to 208 MSPS.

![Fig. 10 Settling time.](image)

![Fig. 11 Full scale current output.](image)

Fig. 11 shows the differential current output of DAC from ‘0000000000’ to ‘1111111111’. The result shows that DAC output is monotonic when the output signal magnitude always increases as the input digital incease.

![Fig. 12 DNL and INL.](image)

Fig. 12 shows the DNL and INL performance of the DAC. The results show that DNL is better than ±0.3 LSB and INL is between ±0.4 LSB which suit for the specification of DAC.

![Fig. 13 output spectrum at 50 MHz, 160 MSPS.](image)

Fig. 13 shows the output spectrum for a 50 MHz input signal at a 160 MHz conversion rate and the SFDR is 68.8 dB.

![Fig. 14 Microphotograph of the realized chip.](image)

Fig. 14 shows the microphotograph of the realized chip. The chip area is 1.73 mm × 1.2 mm and the power dissipation is 45.3 mW at a sampling frequency of 160 MSPS with 2.5-V power supply. Table I shows the summarize results of the propose DAC.

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<th>TABLE I PERFORMANCE SUMMARY</th>
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<td>Power Supply</td>
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VI. CONCLUSION

A segmented 8 + 2 current steering DAC has been presented. The designed DAC can operate at a sampling frequency of 160 MHz and above with 10-bit resolution. The prototype was fabricated by using TSMC 0.25 um 1P5M CMOS technology and it acquired an area of 1.73 mm × 1.2 mm. The power dissipation of the DAC is 45.3 mW with 2.5 V power supply.
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REFERENCES


