A Low Power and Low Phase Noise Complementary Colpitts Quadrature VCO


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Abstract — A low power and low-phase noise quadrature voltage controlled oscillator (QVCO) using the differential complementary Colpitts oscillator topology has been developed. A transformer inductor is used to form a differential output oscillator and the back-gate coupling technique is used to generate quadrature outputs. The advantage of proposed QVCO is analyzed in terms of power consumption, phase noise, and figure of merit. The low power QVCO has been fabricated with 0.18um CMOS technology for 4.8GHz band operation and its phase noise is -115.24 dBc/Hz at 1MHz offset while operated with 2.2mA current consumption and 3.96mW power consumption for the whole QVCO from 1.8V supply. The figure of merit is -182.2 dBc.

Key Words — CMOS, Colpitts oscillator, quadrature, voltage controlled oscillator, back-gate coupling, transformer.

I. INTRODUCTION

The study of direct conversion radio transceivers has dramatically increased in recent years due to the need for low-power, low-cost, and highly integrated transceiver chips, and these direct conversion architectures require quadrature voltage controlled oscillator (QVCO) signals. There are several design options [1] available to generate the QVCO signals: These are 1) combination of VCO, polyphase-filter and output buffers , 2) VCO at double frequency followed by master slave flip flops, and 3) two cross-coupled VCOs, 4) superharmonic coupling, 5) transformer coupled quadrature VCOs, and 6) quadrature VCO with back-gate coupling[2]. Each method has its own merits.

In this paper, we propose a new low power and low phase noise quadrature VCO circuit. We use the coupled inductor concept to form a differential complementary (C-) Colpitts VCO, which can effectively improve the phase noise [3]. Then we use this differential VCO cell to construct a low power QVCO with the back-gate coupling technique.

II. DIFFERENTIAL C-COLPITTS OSCILLATOR

Figs. 1 (a) and (b) [4] show the complementary (C-) Colpitts oscillator and the equivalent small-signal circuit, respectively. In Fig. 1(b), Gm = gmn + gmp, Cgs, Csub, and Rsub represent the overall transconductance, the overall gate-source capacitance, the drain to substrate parasitic capacitance and the resistance of the transistors MN1, and MP1 in Fig. 1(a), respectively. R1 represents the series resistance of inductor L1. gmn and gmp are respectively the transconductances of MN1 and MP1.

Fig. 1(b) is a standard small-signal equivalent circuit of a Colpitts oscillator, which has a tap between two capacitors. The oscillator [4] core is composed of only two components: a complementary pair of transistors and one inductor, and is adequate for high frequency, low noise, and low power application, due to the simplicity and the high negative conductance of the oscillator core.

Fig. 2 shows the proposed differential C-Colpitts oscillator, which uses the concept of inductor coupling. k is the coupling coefficient, L1 and L2 are the transformer inductors. As described in [3], for all reciprocal coupling topologies, the total phase noise is reduced provided the coupling phase is chosen correctly. Following this rule, two complementary Colpitts oscillators can be coupled with each other. In doing so, two advantages are obtained. First, the two complementary Colpitts oscillators are locked together and the output signals are differential. Second, due to coupling effect, the phase noise will be reduced. Compared to Fig.4(b) in [5], the proposed circuit use less active devices, therefore the circuit has the potential of low power and low cost due to less chip occupied area. In addition, one transformer instead of two inductors is used, and the chip area can be further scaled down.

There are many ways to construct a QVCO based on the proposed cell in Fig. 2. We choose the back-gate coupling [2] approach as a mechanism. Fig. 3 shows the implemented quadrature VCO schematic with the output buffers (not shown). It integrates two differential C-Colpitts oscillator proposed in Fig. 2 and based on the back-gate coupling structure to form the quadrature output signal. The circuit is formed by four pairs of NMOS (MN1, MN2, MN3 and MN4) transistors and PMOS (MP1, MP2, MP3 and MP4) transistors, and the overall Cgs, the overall Csub and the resistance of the...
transistors. L1 and L2, and L3 and L4 are transformer inductors. All transistors are housed in separate wells, so that each transistor can be used as a full four-terminal device. The resistors Rb are added for dc biasing of the body terminals and the capacitors Cb for ac coupling. The two differential VCOs are coupled through the back-gates of the core NMOS (MN1, MN2, MN3 and MN4) transistors. The capacitors Cv are implemented with the accumulation mode varactors to control the resonant frequency of the complementary Colpitts QVCO, they are in series with MIM capacitance Cm. The capacitors Cf between gate and source of NMOS transistors are an extra design parameter which can be used to reduce the phase noise and to enhance the start-up of oscillation. The QVCO requiring no additional active components to couple each other has several advantages: First, without any active coupling components, the noise source reduced and phase noise of the oscillator decreased. Secondly, without those coupling components, the chip area will be reduced and the power dissipation reduces. The QVCO circuit has been simulated with the circuit simulator Spectra-RF to provide a quadrature signal output.

### III. EXPERIMENTAL RESULT

This circuit shown in Fig. 3 is implemented in a standard triple-well 0.18um CMOS technology for 4.5GHz operation band. Fig. 4 shows the microphotograph of the fabricated chip.

On-board measurements of output spectrum and output power performances were obtained using an Adventest R3162 spectrum analyzer. Fig. 5 shows the output spectrum at 4.84 GHz, with -6.88 dBm output power for the circuit with operated current of 2.2 mA from 1.8-V supply with the power dissipation of 3.96mW. The phase noise of the QVCO is -115.24 dBc/Hz at 1MHz offset frequency. Fig. 6 shows the frequency tuning range versus varactor control voltage (Vcon) tuned from 0 to 1.8V, and the output frequency is from 4.39 GHz to 4.88 GHz. The capacitors Cv are made of accumulation-mode MOS as Vcon increased, its average capacitance per oscillation cycle decreases, the oscillation frequency therefore increases. Table I summarizes the measurement results at 4.8GHz operation.

The QVCO is compared to other recently published VCOs in Table II using the figure of merit defined as [8].

\[
FOM = L(\Delta \nu) + 10 \log\left(\frac{\Delta \nu}{f_{\text{osc}}}\right)^2 \cdot P_{\text{DC}}
\]

where \(L(\Delta \nu)\) is SSB phase noise measured at \(\Delta \nu\) offset from \(f_{\text{osc}}\) carrier frequency and \(P_{\text{DC}}\) is DC power consumption in mW. As shown in Table II, the figure of merit (FOM) of the quadrature VCO is -182.2 dBc and is the lower value among the previously reported quadrature VCO.

### IV. CONCLUSION

A new low power and low phase noise complementary Colpitts quadrature voltage control oscillator with coupled inductors and back-gate coupling topology based on 0.18-um triple-well CMOS technology has been developed. The implemented C-Colpitts QVCO shows phase noise of -115dBc/Hz at 1-MHz offset while dissipating only 2.2 mA for the whole C-Colpitts QVCO from the 1.8-V supply. The frequency tuning range of the quadrature VCO is from 4.39GHz to 4.88GHz. And the figure of merit of the VCO is -182.2 dBc and is the lower value among the previously reported quadrature VCO.
ACKNOWLEDGEMENT

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REFERENCES


TABLE I

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<tr>
<th>Parameter</th>
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<td>Supply Value</td>
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<td>Oscillator Core Current</td>
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<tr>
<td>Power Consumption</td>
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<td>Frequency Tuning Range</td>
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<td>Frequency VCO Gain</td>
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<tr>
<td>QVCO Frequency</td>
<td>(4.867GHz) VCO in 1MHz -115.24dBc/Hz</td>
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TABLE II

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Fig. 5. Output spectrum of the QVCO at 4.8 GHz

Fig. 6. Output frequency versus control voltage